Accuracy and Power Tradeoff in Spike Sorting Microsystems with Cubic Spline Interpolation

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***Abstract*—Accurate spike sorting is an important issue for neuroscientific and neuroprosthetic applications. The sorting of spikes depends on the features extracted from the neural waveforms, and a better sorting performance usually comes with a higher sampling rate (SR). However the long duration experiment on free-moving subjects is the current trend. For low power considerations, the compromise on sorting accuracy is made for the miniaturized and wireless neural recording ICs with a lower SR. In this paper, we introduce the cubic spline interpolation to strike the power and accuracy tradeoff on the recording microsystems for the off-site and on-chip spike sorter. According to the simulation results, the recorder operated with the SR of 12.5k sample per second (sps) outperforms the system with 25ksps SR on both accuracy and power if the interpolation is appropriately performed before the spike sorting.**

I. Introduction

Spike sorting is an important tool to study neural activities and brain functions in neuroscience research. It is also a key component in cortically-controlled neuroprosthetics for spinal cord injured patients. Robust sorting performance is a critical issue for these applications [1]. The results of the neural decoding is less significant without an accurate spike sorting. However making miniaturized and wireless microsystems for the experiments on free-moving subjects is the current design trend. On these resource-constrained systems, the design issues for low power consumption is usually considered and may result in the compromise on sorting performance.

One of the design issues for the power and accuracy tradeoff is the sampling rate in the neural recorder. Since the classification of spikes depends on the features extracted from the spike waveforms, a better sorting performance usually comes with a higher sampling rate. However the high sampling rate leads to a larger power consumption for the neural recording circuitry, which may not be feasible for the applications. A sampling rate of 100k sample per second (sps) is suggested in [2] for an excellent performance. However the current microsystems are usually designed with 25–40ksps sampling rates [3].

In this paper, we introduce the cubic spline interpolation in order to strike this tradeoff between power and accuracy. Since most spike energy is under 6.25kHz [2], the sorting performance with 100ksps signal resolution could be achieved even with a low sampling rate and low power consumption for the neural recorder after the waveform reconstruction through the interpolation. The remainder of this paper is organized as follows. The preliminary information is described in Section II. In Section III, the interpolation is applied to the neural recording systems with off-site and on-line spike sorter. Section IV demonstrates the improvement on power and accuracy, and Section V describes the conclusion and future works.

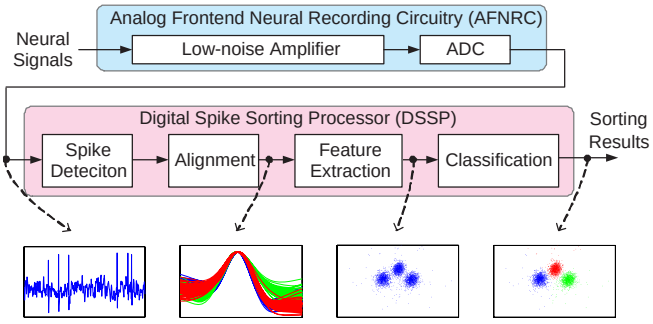


Fig. 1. The hardware operation of the neural recording and spike sorting.

II. Preliminary

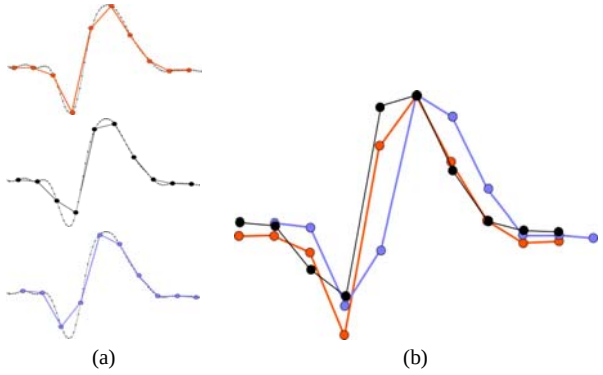
A. Spike Sorting

Most neurons in the brain communicate by firing action potentials, or spikes. These electrical voltage signals can be recorded extracellularly with very thin electrodes implanted into brains. Very often an implanted electrode records the signals from multiple surrounded neurons, and the recorded waveform is the superimposed potentials fired from these neurons. Spike sorting is a kind of reverse process to differentiate which spike corresponds to which of these close-by neurons from the superimposed waveform.

Figure 1 shows the hardware operations of the neural recording and the spike sorting. The analog frontend neural recording circuitry (AFNRC) digitizes the signals after the amplification and filtering of the microvolt neural potentials. Afterwards, the neural samples are input to the digital processor for the spike sorting. The spikes are detected according to their localized instantaneous energy. Then the waveform characteristics, or the features, of the spikes are extracted after the waveform alignment. Spikes with similar features should be corresponding to a specific neuron. Therefore, the spikes are classified according to the assembled clusters on the finite-dimension feature space.

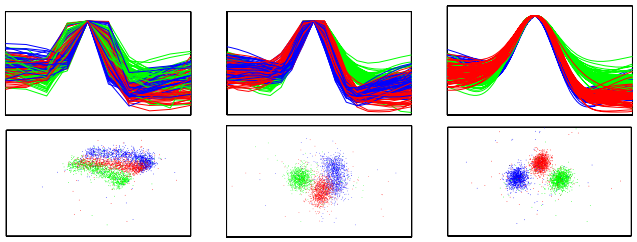
B. Sampling Skew and Waveform Distortion

During the spike sorting, the extracted features of spikes are correlated to the shapes of the spike waveforms. As a result any waveform distortion may have great influence on the performance of spike sorting. Sampling skew is one of the main issues resulting the waveform distortion. During the neural recording, the firing of the action potentials can hardly be synchronized with the sampling of the neural signals. Different time skews corresponding to the neural firing time are sampled for different spikes. Therefore, the variation of



(a) (b)

Fig. 2. The waveform distortion caused by the sampling skew.



(a) (b) (c)

Fig. 3. The improvement of neuron cluster separation after the interpolation. The original neural signals are sampled at 12.5ksps as shown in (a). For (b) and (c), the spike waveforms are re-aligned after the up-sampling to 25ksps and 100ksps with cubic spline interpolation. The principal component analysis are performed after the wavelet transformation for the feature extraction. Since the synthesized neural data from [4] are used, different colors corresponding to different neurons are drawn according to the golden standards (not the classification results).

the spike waveforms are created and results in the degradation of the sorting performance.

Figure 2 demonstrates the waveform distortion caused by the sampling skew. Three spikes generated by the same neuron are shown in Fig. 2 (a). The background waveforms are sampled at the rate of 100k sample per second (sps), while the foregrounds are sampled at 12.5ksps. Since most of the spike energy (ex. 92.5% [2]) has frequency response under 6.25kHz, the sampling frequency of 12.5ksps should be feasible to preserve most spike information for sorting. However, because of the sampling skew, significant differences between three spikes at 12.5ksps are displayed in Fig. 2 (b) after the waveform alignment along the amplitude peaks. The most obvious distortions were happened in the neural polarization and depolarization regions (i.e. peak and valley) which are the most significant waveform characteristics used for spike sorting.

C. Power and Accuracy Tradeoff

A common solution for the sampling skew is to increase the sampling frequency. The sample rate of 100ksps is suggested in the system requiring high-end sorting performance [2]. However, portable or implantable neural recorders supporting a large channel number and wireless functionality [3] are the current trend for the experiments on freely moving subjects. Low power consumption is essential for the implantable devices. Low data rate may also be required for the wireless telemetry under limited hardware resources. The systems with high sampling rates usually result in a large power consumption and high data rate, and is not feasible for the

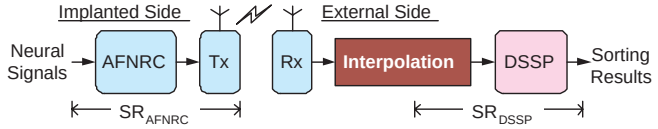


Fig. 4. The proposed off-site spike sorting system with interpolation. SR_{AFNRC} and SR_{DSSP} indicate the sampling rates of the processed data in AFNRC and DSSP respectively.

applications. Therefore, the sampling rates of 25–40ksps are generally adopted in the current hardware prototypes with the compromise on the accuracy of spike sorting [3].

D. Interpolation

The spikes have the most energy under 6.25kHz. According to the Nyquist-Shannon sampling theory, it should be feasible to reconstruct the 100ksps spike waveforms through the interpolation if the sampling rate in the AFNRC is higher than 12.5ksps. An uncompromised spike sorting performance may thus be achieved even with a sampling rate as low as 12.5ksps. Figure 3 shows the improvement of the neuron separation by means of the interpolation. The neural signals are originally sampled at 12.5ksps. Then the spike waveforms are interpolated to 25ksps and 100ksps in Fig 3 (b) and (c) respectively. After the interpolation, the spike peaks are reconstructed, and the waveform can be re-aligned with less error caused by the sampling skew. This improves the separation of neuron clusters on the feature space and leads to a better sorting performance.

III. Spike Sorting Systems with Interpolation

The spike sorting systems can be divided into two categories—the off-site spike sorter and on-chip spike sorter. In this chapter, we will describe how to improve the power and accuracy tradeoff through the interpolation in these two systems.

A. Proposed Off-site Spike Sorter with Interpolation

Figure 4 shows the wireless neural recorder along with the off-site spike sorter. After the wireless transmission, the spike sorting is operated on the external devices where the hardware resources may somehow be considered unlimited. The limited power is consumed by the AFNRC and wireless transmitter. According to the previous discussion, there is a tradeoff between the accuracy and power in this framework. If the whole system is operated at 100ksps signal resolution (i.e. $SR_{ADNRC} = SR_{DSSP} = 100ksps$), the implanted side will consume significant power because of a large data rate. The power can be saved with the compromise on the sorting accuracy if a lower signal resolution is adopted.

The interpolation can be utilized to improve the power-accuracy tradeoff. In the proposed system, the spike sorting is performed after the reconstruction of the high-resolution neural signals in the external side. Two kinds of improvement can be expected along the power and accuracy axis. With a fixed sampling rate and power consumption in the implanted side, our system achieves a higher sorting accuracy after the interpolation. With an expected sorting accuracy, the implanted side may consume lower power consumption with a lower sampling rate because the compensation can be made by the interpolation in the external side .

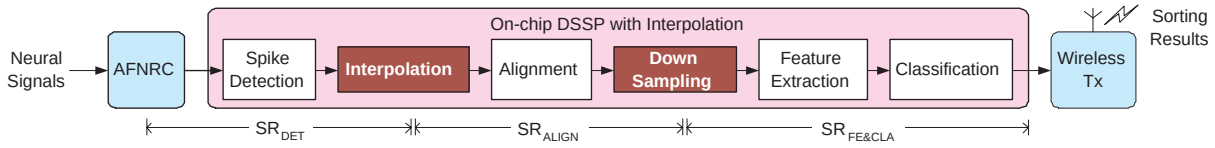


Fig. 5. The proposed on-chip spike sorting system with interpolation. The SR_{DSSP} here can be further divided into SR_{DET}, SR_{ALIGN}, and $SR_{FE\&CLA}$ representing the data sampling rates of spike detection, alignment, and feature extraction along with classification stages.

B. Proposed On-chip Spike Sorter with Interpolation

The wireless neural recorder with on-chip spike sorter transmits only sorting results which have significantly reduced data rate compared to the raw data [1]. Therefore more channel number can be supported or a lower-end wireless transmitter with smaller power can be utilized. The on-chip spike sorter will also be a critical component in the implantable realtime cortically controlled neuroprosthetics [1]. Since only the sorting results are transmitted and there is no room to manipulate the waveform for accuracy improvement in the external side, the interpolation process is introduced on chip. The power consumption is still an important issue here. Although the usage of the interpolation increases the power of DSSP, it would release the requirement of the high sampling rate of AFNRC in some respects. Since the power consumed by the AFNRC chips [3] is about an order larger than the state-of-the-art DSSP designs [5], this power tradeoff between the AFNRC and DSSP would finally result in a smaller total power.

The DSSP consumes larger power after the interpolation. This penalty can be minimized if the high signal resolution is only utilized at the critical step of the spike sorting. Figure 5 shows the system with the proposed on-chip spike sorter. The DSSP part is divided into three sections with the specific purposes. First the spike detection usually uses the energy detector and does not need detailed waveform information. Therefore the SR_{DET} along with the SR_{AFNRC} should be set as low as possible in order to save power. Afterwards, the interpolation is performed and the detected spikes are aligned with a higher SR_{ALIGN} in order to reduce the sampling skew and improve the ability of neuron separation. After the alignment, the feature extraction and classification, the most computationally intensive parts of spike sorting, are operated after the down-sampling. Since the sampling skew is minimized during the high-resolution alignment, there should be limited waveform distortion after the down-sampling and the sorting performance is kept with lower power consumption.

IV. Simulation Results and Discussion

A. Simulation Environment

1) Neural Data and the Algorithms: The neural signals from [4] are the 25ksps spikes recorded from the neocortex and basal ganglia along with the superimposed background noise. For the spike sorting algorithm, the nonlinear energy operator (NEO) [6] is adopted in the spike detection. Afterwards the spike windows are aligned vertically (along amplitude axis) and horizontally (along time axis) according to the first waveform peak. During the feature extraction, principal component analysis (PCA) are performed after the discrete Haar wavelet transformation for the aligned spikes. Finally, the classification based on the Watersheds segmentation algorithm [7] is used to sort the spikes on the feature space.

TABLE I
Comparison between Different Interpolation Filters

	Unit	Neural Data #a (nd.a)			Neural Data #b (nd.b)		
SR_{AFNRC}	ksps	12.5	12.5	12.5	12.5	12.5	12.5
SR_{DSSP}	ksps	25	50	100	25	50	100
Bilinear	CSP	0.61	0.76	0.99	1.37	1.41	1.43
Cubic Spline	CSP	1.69	1.91	1.99	1.63	1.95	2.06

As for the interpolation, the cubic spline algorithm is mainly used to test our system while the bilinear filter is also simulated as a reference. The cubic spline algorithm is based upon solving the piecewise polynomials for the continuous first and second derivatives, and is able to reconstruct the waveform peak and valley with smaller error compared to the bilinear interpolation.

2) Objective comparison schemes: Although the improvement of the neuron separation can be visually recognized as shown in Fig. 3, two kinds of objective scores are adopted for the comparison and analysis. The first method is to quantify the separation of the neuron clusters on the feature space. In this case the golden standards are directly used as the sorting results. The cluster separation parameter (CSP) as the criterion is defined as follows:

$$CSP = \frac{\Sigma(Mahalanobis\ distances\ between\ a\ pair\ of\ clusters)}{\Sigma(Mahalanobis\ distances\ within\ one\ cluster)}$$

The system with a larger CSP value indicates a better capability for neuron separation. The second method is to run the complete spike sorting algorithm and then compare the results with the golden standards. The matching scores (MS) for spike detection (SD) and spike sorting (SS) are defined as follows:

$$MS_{SD} = \frac{Correctly\ Detected\ Spikes}{Total\ Detected\ Spike} \quad MS_{SS} = \frac{Correctly\ Sorted\ Spikes}{Total\ Detected\ Spike}$$

B. Simulation Results

1) Interpolation Filter: Table I shows the CSP comparison between cubic spline and bilinear interpolations. We use the off-site spike sorter as the simulation platform. The cubic spline filter can reconstruct the peak and valley of spike waveforms, which is important in waveform alignment to reduce the sampling skew error. Therefore the cubic spline interpolation significantly outperforms the bilinear one.

2) Off-site Spike Sorter with Interpolation: Figure 6 (a) shows the CSP comparison between different off-site spike

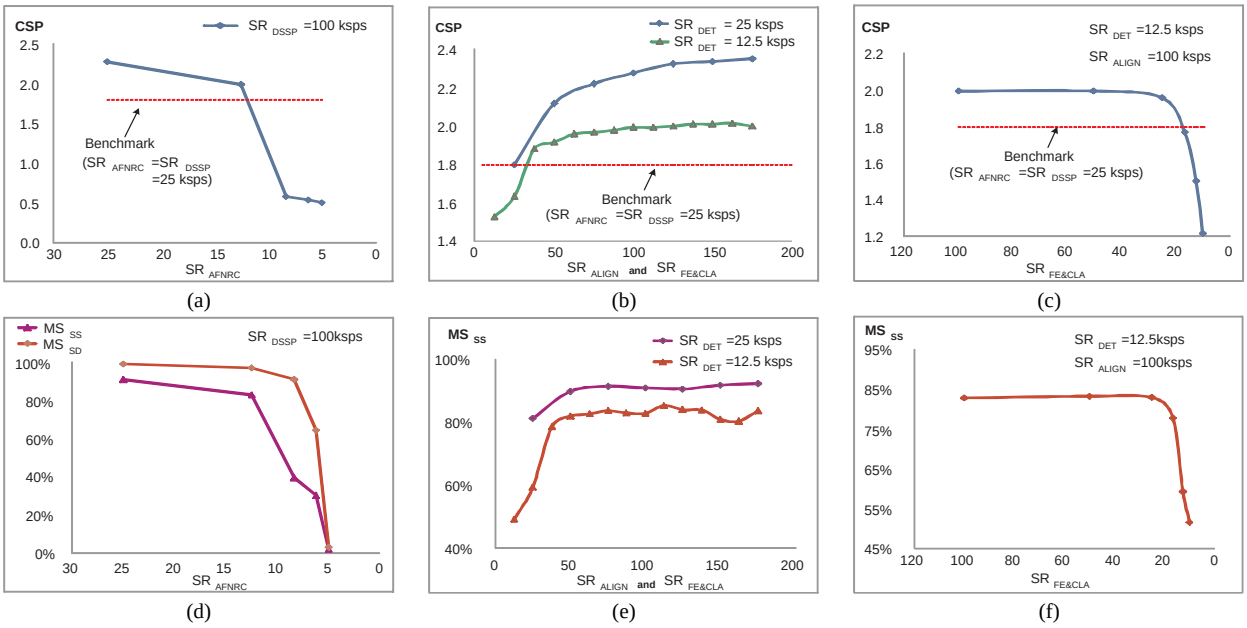


Fig. 6. CSP and MS comparisons of (a,d) off-site spike sorting systems with a fixed SR_{DSSP}; (b,e) on-chip spike sorting systems with a fixed SR_{DET}; (b,f) on-chip spike sorting systems with a fixed SR_{DET} and SR_{ALIGN}.

sorters. Because the external side is supposed to have unlimited power, we fix the SR_{DSSP} at 100ksps. The implant side consumes lower power with a lower SR_{AFNRC}. The results show that the performance rapidly degrades if the sampling rate in AFNRC is less than 12.5ksps. In addition, the system with 25ksps SR_{AFNRC} slightly outperforms that with 12.5ksps. That is because 92.5% spike energy is under 6.25kHz while still 6.6% is between 6.25 and 12.5kHz [2]. The red dotted line in the figure indicates the CSP value of the benchmark system. This benchmark is simulated with 25ksps for both SR_{AFNRC} and SR_{DSSP}. Compared with the benchmark, the system operated at 12.5ksps and 100ksps for SR_{AFNRC} and SR_{DSSP} has a better sorting accuracy and consumes less power in the implant side.

Figure 6 (d) shows the same comparison with MS values. The results demonstrate the same trend as those in the CSP comparison. Note that as SR_{AFNRC} decreases, the rapid falling of MS_{SS} appears faster than that of MS_{SD}. This is because the spike sorting requires the subtle waveform information while the spike detection checks only the energy variation.

3) On-line Spike Sorter with Interpolation: Figure 6 (b) and (c) show the CSP comparisons between different on-line spike sorting systems. According to the analysis in Section IV-B2, the spike detection is less sensitive to the signal resolution. Therefore, we first fix the SR_{DET} to either 12.5ksps or 25ksps. In Fig. 6 (b), we increase the signal resolution before the alignment in order to reduce the sampling skew. The CSP curve begins saturating around 50ksps and slightly increases before 100ksps. In Fig. 6 (c), since spikes are aligned at 100ksps and the sampling skew error is minimized, we can perform the feature extraction and classification in a lower resolution in order to save the power. A flat region is observed when the down-sampling starts. The CSP value rapidly decreases after 25ksps. Compared to the benchmark system, 25ksps, 100ksps, and 50ksps are suggested for SR_{DET}, SR_{ALIGN}, and $SR_{FE\&CLA}$ for an extremely better sorting performance with additional power in DSSP. The system with 12.5ksps, 50ksps, and 25ksps should have less power consumption and still outperform the benchmark. The same comparisons done with MS values are shown in Fig. 6 (e) and (f), and have similar results.

V. Conclusion and Future Works

In this paper, the off-site and on-chip spike sorting systems with cubic spline interpolation is proposed to strike the tradeoff between the sorting accuracy and power consumption. The simulation results show that the 12.5ksps recorder could outperform the 25ksps one on both accuracy and power if the interpolation is appropriately performed before the spike sorting. In the future, the hardware implementation of the cubic spline interpolation is required to complete the proposed system with the on-chip spike sorter.

References

[1] M.D. Linderman and et al., "Signal processing challenges for neural prostheses," *IEEE Signal Proc. Mag.*, vol. 25, no. 1, pp. 18–28, 2008.

[2] T. J. Blanche and N. V. Swindale, "Nyquist interpolation improves neuron yield in multiunit recordings," *J. of Neurosci. Methods*, vol. 155, no. 1, pp. 81–91, 2006.

[3] R. R. Harrison and et al., "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE J. Solid State Circuits*, vol. 42, no. 1, pp. 123–133, 2007.

[4] R. Quian Quiroga and et al., "Unsupervised spike detection and sorting with wavelets and superparamagnetic clustering," *Neural Comput.*, vol. 16, pp. 1661–1687, 2004.

[5] T.-C. Chen and et al., "128-channel spike sorting processor with parallel-folding structure in 90nm process," in *Proc. of IEEE Int. Symp. on Circuits and Syst.*, 2009.

[6] K. H. Kim and S. J. Kim, "Neural spike sorting under nearly 0-db signal-to-noise ratio using nonlinear energy operator and artificial neural-network classifier," *IEEE trans. on Biomed. Eng.*, vol. 47, no. 10, pp. 1406–1411, 2000.

[7] D. Wang, "Unsupervised video segmentation based on watersheds and temporal tracking," *IEEE trans. on Circuits Syst. on Video Technol.*, vol. 8, no. 7, pp. 539–546, 1998.